High electric field transport effects on low temperature operation of pseudomorphic HEMTs

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Abstract

High electric field effect in very small pseudomorphic High Electron Mobility Transistor (HEMT) $Al_{0.22}Ga_{0.78}As/In_{0.2}Ga_{0.8}As/GaAs$ and their influence at low temperature are investigated for $0.1\mu m$ up to $0.4\mu m$ gate lengths. The extent of transport improvement at low temperature and performance degradation associated with gate length reduction are underlined. Limitations in performance improvement appear at low temperature due to trapping effects and to an enhancement of the mechanisms responsible of short channel effects. In pulsed drain operation the evolutions of drain current versus time in the $10ns-600\mu s$ range illustrate the influence of trapping centers and self heating of the lattice in the device. We analyze the variation of gate current versus temperature at high drain bias (>3V) and the influence of impact ionization.

Introduction

Low temperature investigations of III-V semiconductor heterojunction field effect transistors (HEMTs) have mainly focused on the improvements of high frequency performances and low noise operation [1]. We have shown that it is now possible to perform accurate high frequency characterization of HEMTs on wafer in a cryogenic environment, and follow the evolution of their HF electric parameters versus gatelength, temperature, gate and drain bias voltages [2]. We have also pointed out that pseudomorphic HEMTs (PMHEMTs) on GaAs keep very attractive performances in low drain bias conditions which allows low power dissipation in cryogenic conditions [3]. The high electric field gradients bring improvements due to very non stationary (quasi-ballistic) transport. But in the very short gate devices which are now realized, the combined effect of very high electric field and high current density in the device channel may also bring several detrimental features which are related to short channel effects [4],[5],[6], trapping centers [7], impact ionization, self heating in the channel of large current level devices [8]. These aspects have been studied at room temperature. We investigate here how high electric fields influence PM-HEMT properties at low temperatures in $Al_{0.22}Ga_{0.78}As/In_{0.2}Ga_{0.8}As/GaAs$ devices. Such a kind of high field regime may occur in very small devices at relatively moderate drain voltage Vds (<1V). When drain bias increases, one often obtains a smaller output conductance and gatedrain capacitance, which gives a higher maximum oscillation frequency Fmax, a desired feature in circuit

applications. On the other side the gain current cut-off frequency Ft which characterizes carrier transport in the channel and its control by the gate may decrease due to an increasing capture rate on the deep levels, and self heating of the lattice in the active layers. We investigate here these different phenomena versus temperature in order to try to separate their respective contributions. We first describe the device structure and the conditions of experimental characterizations. Then we discuss the origin of the very high electric fields which occur in the devices at moderate biases.We show that the highest frequency performances are obtained at smaller drain voltage when the gatelength and the temperature are reduced.

Experimental conditions

The PM HEMTs represented in Fig.1 are Si-delta-doped ($4.10^{12}m^{-2}$), single-recessed PM-HEMTs with a distance between metal gate and channel a=15nm including a 3nm n.i.d. spacer, a 12nm strained InGaAs channel, gate lengths 0.4µm, 0.3µm, 0.2µm, and 0.1µm.
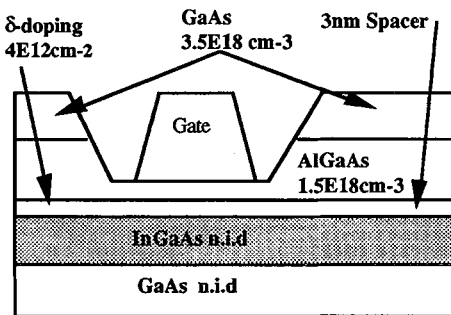

Fig.1: Schematic structure of the device

For each transistor and at each temperature, a DC characterization is achieved to obtain the main extrinsic parameters. A pulsed I-V measurement system involving proper impedance matching conditions and a rise time of 2ns allows to follow the evolution of HEMT drain current beyond a few ns for pulse lengths up to several hundredth µs. A duty cycle of 1/100 maintains negligible the average heating of the lattice. In this way we extend III-V device I-V transient characterization from the usual time scale > 200ns [9] down to a few nanoseconds. This gives new informations on trapping effects in the AlGaAs layer in high electric field conditions, which must be differentiated from possible self-heating effects. Electrothermal simulations show that the latter may become significant in these very high current density devices and originate at the drain side of the gate due to the very high electric fields. Accurate HF measurements up to 40GHz versus temperature using an original cryostat with in-situ calibration [10] are also performed on these state of the art performance devices. All measurements are carried out under illumination to minimize trapping in source and drain access areas under the heavily doped cap layers.

Results and Discussion

The evolution of the output conductance Gd and of the threshold voltage Vth characterize the so called short channel effects in a given HEMT technology. An important shift of Vth towards more negative values and an accompanying increase of Gd when lg is reduced are signatures of the drain voltage influence on the carriers under the gate. These two features are strongly correlated with the drain current saturation mode

and the strong field gradients in these ultrashort gatelength devices. Current saturation occurs partly due to channel depletion and also due to carrier velocity saturation. At the gate end on the drain side, simulations show that such HEMTs may sustain electric fields reaching several hundreds kV/cm. In very short gate devices both the transverse and longitudinal electric field components control the carrier density and their kinetics. Another consequence of short channel effects is the reduction of transconductance when the gate length reduction goes beyond a certain threshold (50-150nm gatelength, depending on technologie). However there may be an interfering effect in this analysis due to the gate recess. In the shortest gate HEMTs, limitation in the control of etching rate of a very narrow recess and overestimation of its depth depth may contribute to a negative Vth shift when lg≈0.1μm.

The fabricated PM-HEMT have DC characteristics which show a negative threshold voltage shift at a given temperature (≈-0.3V) in current saturation regime versus gatelength from 0.4μm down to 0.1μm.Then the devices have relatively moderate short channel effect by virtue of the combined effect of the heterojunction barriers on both sides of the InGaAs quantum well and of the large gate aspect ratio which is still equal to 5 at l_g = 0.1μm. The Vth shift versus temperature is ≈-100mV. The HF output conductance G_d (G_d=30mS/mm for l_g=0.4μm) improves sligthly at smaller lg thanks to the potential barrier between the channel and the substrate.

Fig. 2-3 present pulsed I-V drain current measurements at two DC gate biases (Vgs=0V, Vgs=+0.6V). The drain current amplitude Ids is measured 10ns after the beginning of the drain pulse, 600ns after the beginning of the pulse and when a steady state is reached (Ids(1ms)=Ids(DC)). The reduction of Ids versus time results from the capture of carriers by trapping centers and from an increase of lattice temperature in the device and more particularly in the channel.
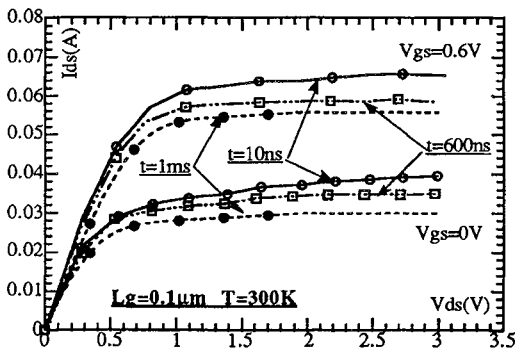

Fig.2: I-V curves of a 0.1μm gate length HEMT at 300K DC measurements and pulsed measurements
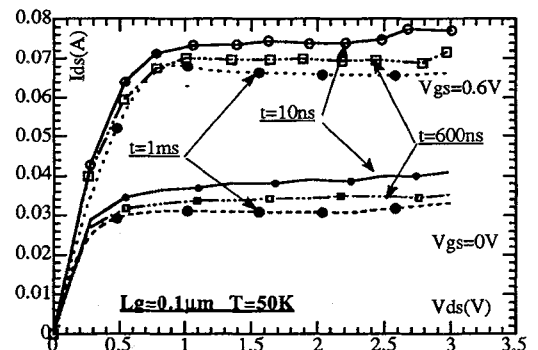
Fig.3: I-V curves of the same device at 50K DC measurements and pulsed measurements

The maximum electrical power dissipated in the device reaches 1.8 W/mm, at Vgs=0.6 V and Vds=3V. Then the lattice temperature estimated using the temperature dependence of the Schottky gate current is about 370 K while holder temperature is 293K. Such an increase of temperature should degrade the drain current. A current transient associated with self heating of the lattice should depend on the power dissipated in a device. The Fig.2-3 show the variations between the 10ns current and the 1ms current amplitude at Vgs=0V and at Vgs=0.6V. The evolution of current amplitude versus time at different dissipated power levels do not show clear evidence of device temperature variations. Then trapping on the deep levels is probably the main mechanism responsable of the observed current transients at least at

moderate power level (e.g. at bias Vgs=0V, Vds=1V). There is no obvious difference between 300K curves and low temperatures ones. The current transients have an approximate exponential form with a large variation in the first few hundreds of ns and a slower evolution until 500µs. The mechanism of capture seems to be largely independent of the holder temperature. This may be explained by the high energy of hot electrons. Then, the apparent cross section of the trapping centers increases due to the high energy of the carriers, because they can overcome easily the deep level potential barrier. On the other side, it must be noted that the emission time is strongly temperature dependent and becomes very large compared with the duration of the measurements at low temperature. The complexity of the above dynamic characterizations will require further detailed time domain investigation to clarify the respective time scales and consequences of trapping centers and self heating,
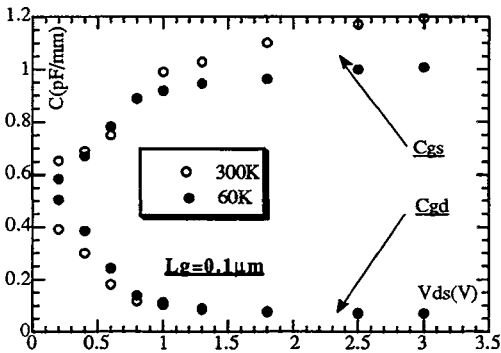
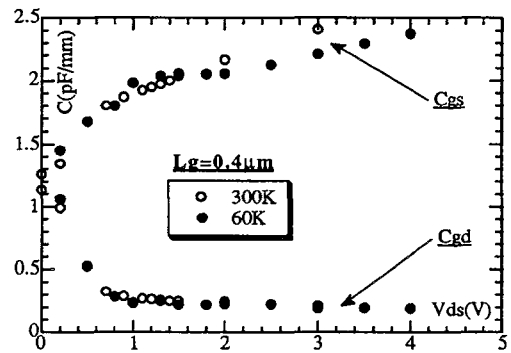Fig. 4: Capacitances Cgs and Cgd versus Vds for a 0.1µm gate length HEMT at T=300K and T=60K

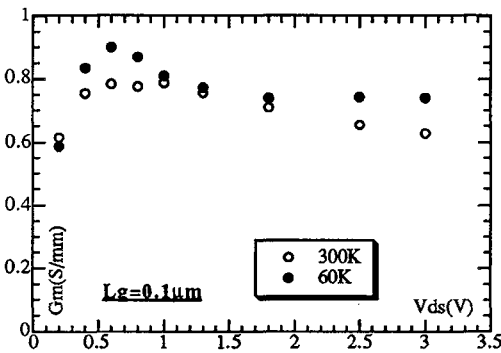Fig. 6: Capacitances Cgs and Cgd versus Vds for a 0.6µm gate length HEMT at T=300K and T=60K

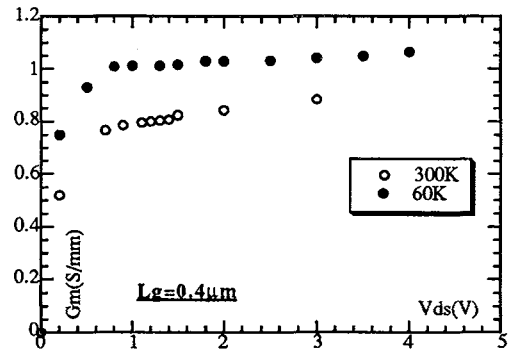Fig. 5: Transconductances Gm versus Vds for a 0.1µm gate length HEMT at T=300K and T=60K

Fig. 7: Transconductances Gm versus Vds for a 0.4µm gate length HEMT at T=300K and T=60K

The evolution of the high frequency transconductances gm and the capacitances of a 0.1µm and 0.4µm gate length devices versus drain bias at two temperatures T=300K and T=50K are presented in Fig.3-7. One may underline the general improvement of gm upon cooling, even if the Cgs capacitance decreases versus temperature at relatively high drain voltage. This is due to trapped electrons which can't be easily reemitted at low temperature. Simulations of the coupled Poisson and Schrödinger equations along the epitaxial growth axis and neglecting trapping centers confirm that the population under the gate

should be nearly the same at 50K and 300K in open channel condition. Therefore electron population should not change significantly under the gate and capacitances should remain nearly constant upon cooling. However carrier trapping at DX centers modifies this scheme.

The transport properties improvement at low temperature are well illustrated by the increase of intrinsic transconductance while the carrier density under the gate decreases. The well known "short channel effect" explains the evolution of the Gm curves between the 0.1μm and 0.4μm gate length device. The former exhibit a maximum at low Vds (Vds=0.7V) while the latter increase steadily with drain voltage. The stronger bidimensional character of electric fields in the shortest device (see above) is enhanced at low temperature due to small dimensions and non stationnary transport. The output conductance increases (20% for 0.1μm gate length device) and the threshold voltage shifts towards more negative value (-100mV for Lg=0.1μm). Then it appears a strong paralellism of high field effects if the gate length is reduced or if the device is cooled.

At any gate bias, there are electrons in the AlGaAs layer at the entrance of the gate owing to lateral diffusion from access area, and these electrons can't be detrapped by light. When increasing Vgs the rate of electrons in the AlGaAs layer under the gate increases and more electrons are trapped. The carriers cannot be reemitted quickly at low temperature and the Cgs capacitance becomes smaller .
There is a dual influence of the drain bias on DX centers population rate. Higher electric fields create higher energy electrons which increases the apparent cross section of the DX centers because electrons may overcome easily the potential barrier before being trapped. On the other side the Poole-Frenkel effect should allow an easier detrapping from the deep level centers.

At higher drain voltage (>3V) the effect of impact ionization appears and has been observe in electroluminescence measurements[11]. Fig 8. shows the effect of impact ionization on the gate current of a PM-HEMT at Vds=0V and Vds=5V and at the temperatures 300K and 20K.
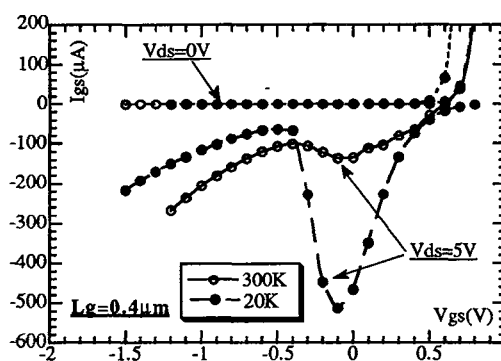

Fig.8 : Gate current of a 0.4μm gate length HEMT
versus Vgs at Vds=0V, Vds=5V, T=300K and T=60K

Above Vds=3.5V the gate current under reverse bias condition of the Schottky gate is enhanced by a hole current which exhibits a maximum and decreases afterwards. This phenomenon is caused by impact ionization. A large fraction of the holes created by ionization drifts towards the source side but part of them cross over the gate potential barrier and are collected by the latter. The shape of the gate current variation at increasingly negative voltages may be understood as follows. First , the hole current intensity increases with the drain-gate voltage. Then near to the HEMT threshold voltage (Vgs=-1V) the channel current

decreases strongly   and the hole current created by impact ionization is reduced . The hole current is enhanced at low temperature due to stronger impact ionization. A fraction of the holes larger than at 300K get enough energy to cross over the barrier and reach the gate.

Consequently a high drain voltage at low temperature results in some reduction of intrinsic carrier transport capabilities of the present PMHEMTs, although some parameters such as the output conductance Gd and the maximal oscillation frequency Fmax are improved or at least remain constant when increasing Vds. We obtain the best Fmax at Lg=0.2μm, a good gatelength trade-off between high transport capabilities, efficient gate control with minimum influence of the drain. The maximum value of Fmax increases from 150GHz at 300K up to 230GHz at T=60K and does not decrease practically at high Vds. This large improvement is due to the strong reduction of access resistances and more particularly Rg (50%), and to the increase of current gain cut off frequency at low temperature.

Conclusion

The overall dc, pulsed and HF measurements show that for best HF performances, it is convenient to operate PM-HEMT at relatively low positive Vgs to avoid a too large DX center influence and parasitic transport in large gap delta doped layers, and at low Vds (0.8V<Vds<1.2V) to limit both self heating of the lattice and trapping of hot carriers in DX centers. The longer gate HEMTs present a stronger improvement of the intrinsic parameters than the shorter ones. Cooling down a device reduces all access resistances and improves transport under the gate. Further optimization of the structure related to the phenomena involved in the gate-drain area at low temperature should be performed to realize smaller output conductance devices at low Vds and obtain a better overlap of their maximum Ft and Fmax.

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