

Allegro® PCB Editor

Version 15.2

Training Manual

Book 1

July 21, 2004

cadence

© 1990-2004 Cadence Design Systems, Inc. All rights reserved.

Printed in the United States of America.

Cadence Design Systems, Inc., 555 River Oaks Parkway, San Jose, CA 95134, USA

Cadence Trademarks

1st Silicon Success®

Allegro®

Assura™

BlackTie®

BuildGates®

Cadence® (brand and logo)

CeltIC™

ClockStorm®

CoBALT™

Concept®

Conformal®

Connections®

Design Foundry®

Diva®

Dracula®

Encounter™

Fire & Ice®

First Encounter®

FormalCheck®

HDL-ICE®

Incisive™

IP Gallery™

Nano Encounter™

NanoRoute™

NC-Verilog®

OpenBook® online documentation library

Orcad®

Orcad Capture®

Orcad Layout®

PacifIC™

Palladium™

Pearl®

PowerSuite™

PSpice®

QPlace®

Quest®

SeismIC™

SignalStorm®

Silicon Design Chain™

Silicon Ensemble®

SoC Encounter™

SourceLink® online customer support

SPECCTRA®

SPECCTRAQuest®

Spectre®

TtME®

UltraSim®

VeriFault-XL®

Verilog®

Virtuoso®

VoltageStorm®

Other Trademarks

All other trademarks are the exclusive property of their respective owners.

Confidentiality Notice

No part of this publication may be reproduced in whole or in part by any means (including photocopying or storage in an information storage/retrieval system) or transmitted in any form or by any means without prior written permission from Cadence Design Systems, Inc. (Cadence).

Information in this document is subject to change without notice and does not represent a commitment on the part of Cadence. The information contained herein is the proprietary and confidential information of Cadence or its licensors, and is supplied subject to, and may be used only by Cadence's customer in accordance with, a written agreement between Cadence and its customer. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information.

RESTRICTED RIGHTS LEGEND Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subparagraph (c)(1)(ii) of the Rights in Technical Data and Computer Software clause at DFARS 252.227-7013.

UNPUBLISHED This document contains unpublished confidential information and is not to be disclosed or used except as authorized by written contract with Cadence. Rights reserved under the copyright laws of the United States.

Contents

| | | |
|------------------|---|------|
| Lesson 1: | Allegro PCB Editor User Interface | 1-1 |
| | Primary Allegro PCB Editor Programs | 1-2 |
| | Other Programs | 1-3 |
| | Cadence SPB Tools | 1-4 |
| | Course Directory Structure | 1-5 |
| | Setting and Changing Your Working Directory | 1-6 |
| | Allegro PCB Editor and Workspace | 1-7 |
| | Toolbar | 1-8 |
| | Control Panel and World View Window | 1-9 |
| | Getting Help | 1-10 |
| | Lab | 1-11 |
| | Lab 1-1: Allegro PCB Editor Tour | 1-12 |
| | Mouse Buttons | 1-18 |
| | Controlling the Window Display | 1-19 |
| | Navigating in the World View Window | 1-21 |
| | Zoom Control Using the Middle Mouse Button | 1-22 |
| | Default Aliases for Function and Control Keys | 1-23 |
| | Running Commands with Strokes | 1-24 |
| | Controlling the Toolbars | 1-25 |
| | Drawing Parameters | 1-26 |
| | Drawing Options: Display and Status | 1-27 |
| | Drawing Options: Line Lock and Symbol | 1-29 |
| | User Preferences | 1-31 |
| | Lab | 1-32 |
| | Lab 1-2: Navigating the PCB Editor User Interface | 1-33 |
| Lesson 2: | Managing the PCB Editor Work Environment | 2-1 |
| | Groups, Classes and Subclasses | 2-2 |
| | More Groups, Classes and Subclasses | 2-3 |
| | Options Window of the Control Panel | 2-4 |
| | Controlling Color and Visibility | 2-5 |
| | Controlling Etch Visibility | 2-6 |
| | Graphics Dimming or Shadow Mode | 2-7 |
| | Scripts | 2-8 |
| | Lab | 2-9 |
| | Lab 2-1: Script Files and Controlling Visibility and Color | 2-10 |
| | The Selectable Objects List | 2-16 |
| | Using the Find by Name Section | 2-17 |
| | Using Find by Property | 2-18 |
| | Highlighting Elements | 2-19 |
| | Using the Show Element Command | 2-20 |
| | Using the Display Measure Command | 2-21 |
| | Labs | 2-22 |
| | Lab 2-2: Highlighting and Using the Find Filter | 2-23 |
| | Lab 2-3: Using the Find Filter with the Show Element Command | 2-29 |

| | | |
|------------------|--|------|
| Lesson 3: | Padstacks | 3-1 |
| | Anatomy of a Padstack | 3-2 |
| | Padstack Details..... | 3-3 |
| | What is a Thermal Relief? | 3-4 |
| | Flash Symbols..... | 3-5 |
| | Lab | 3-6 |
| | Lab 3-1: Creating a Flash Symbol | 3-7 |
| | What Does the Padstack Designer Do? | 3-10 |
| | Padstack Designer - Parameters | 3-11 |
| | Padstack Designer - Layers | 3-13 |
| | Defining Pad Shapes/Sizes..... | 3-14 |
| | Adding/Deleting/Copying Layers | 3-15 |
| | Saving the Padstack..... | 3-16 |
| | Labs..... | 3-17 |
| | Lab 3-2: Creating Padstacks for a Through-Hole Pin Device | 3-18 |
| | Lab 3-3: Creating a Padstack for a Surface- Mounted Device | 3-27 |
| Lesson 4: | Component Symbols | 4-1 |
| | Package Symbol Wizard..... | 4-1 |
| | Drawing Parameters Form..... | 4-2 |
| | Drawing Origin..... | 4-3 |
| | Moving the Drawing Origin..... | 4-4 |
| | PCB Editor Symbol Types..... | 4-5 |
| | Example: a 14-pin DIP Package | 4-6 |
| | Adding Pins | 4-7 |
| | Drawing Component Outlines..... | 4-9 |
| | Adding Labels | 4-10 |
| | Defining Area Constraints..... | 4-11 |
| | Saving Symbol Files | 4-12 |
| | Labs..... | 4-13 |
| | Lab 4-1: Creating a DIP16 Package Using the Package Symbol Wizard..... | 4-14 |
| | Lab 4-2: Creating a DIP14 Package Symbol | 4-18 |
| | Lab 4-3: Creating an SOIC16 with the Symbol Editor (<i>optional lab</i>)..... | 4-29 |
| Lesson 5: | Board Design Files | 5-1 |
| | Creating a Board Symbol..... | 5-2 |
| | Typical Board Outline..... | 5-3 |
| | Drawing a Board Outline | 5-4 |
| | Tooling/Mounting Holes | 5-5 |
| | Chamfers | 5-6 |
| | Linear Dimensioning..... | 5-7 |
| | Defining Constraint Areas (Keepins/Keepouts)..... | 5-8 |
| | Saving Board Symbol Files (.bsm and .dra) | 5-9 |
| | Board Wizard..... | 5-10 |
| | Labs..... | 5-11 |
| | Lab 5-1: Creating a Board Mechanical Symbol | 5-12 |
| | Lab 5-2: Creating a Board using the Board Wizard | 5-30 |
| | Allegro PCB Editors - Overview | 5-33 |
| | Creating a Master Design File | 5-34 |
| | Defining Layer Stackup | 5-35 |
| | Lab | 5-36 |

| | |
|--|------|
| Lab 5-3: Creating a Master Design File (.brd)..... | 5-37 |
| Lesson 6: Importing Logic Information into Allegro PCB Editor | 6-1 |
| Design Layout Process | 6-2 |
| Design Entry HDL-Integrated Logic Design with Physical Layout..... | 6-3 |
| Transfer Files (pst*.dat) | 6-4 |
| Importing Logic into PCB Editor from Design Entry HDL | 6-6 |
| Importing Logic Data..... | 6-7 |
| Engineering Changes—Placement | 6-8 |
| Importing Electrical Constraints..... | 6-9 |
| Engineering Changes—Routing | 6-10 |
| Schematic-Driven Layout..... | 6-11 |
| Design Entry CIS-Integrated Logic Design with Physical Layout..... | 6-13 |
| Design Entry CIS Interface with PCB Editor | 6-14 |
| Design Entry CIS-PCB Editor Logic Import | 6-15 |
| Third-Party Logic Import | 6-16 |
| Netlist Format | 6-17 |
| General Rules for Netlists | 6-18 |
| Device Files..... | 6-19 |
| Package Properties in Device Files..... | 6-20 |
| Loading a Third-Party Netlist | 6-21 |
| Netin Checking | 6-22 |
| Guidelines for Importing Logical Data..... | 6-23 |
| Labs | 6-24 |
| Lab 6-1: Design Entry HDL to PCB Editor..... | 6-25 |
| Lab 6-2: Design Entry CIS to PCB Editor..... | 6-30 |
| Lab 6-3: Importing a Third-Party Netlist..... | 6-33 |
| Lesson 7: Setting Design Constraints | 7-1 |
| Design Layout Process | 7-2 |
| Introduction to Design Rules..... | 7-3 |
| Setting Up Design Rules..... | 7-4 |
| Standard (default) Design Rules | 7-4 |
| Extended Design Rules..... | 7-5 |
| Spacing Rule Set—Step 1..... | 7-6 |
| Spacing Rule Set—Step 2 | 7-7 |
| Spacing Rule Set—Setting Rules by Layer | 7-8 |
| Spacing Rule Set—Step 3 | 7-9 |
| Labs | 7-10 |
| Lab 7-1: Standard Design Rules | 7-11 |
| Lab 7-2: Extended Design Rules—Spacing | 7-13 |
| Physical Rule Set—Step 1 | 7-18 |
| Physical Rule Set—Step 2 | 7-19 |
| Physical Rule Set—Etch by Layer..... | 7-20 |
| Physical Rule Set—Step 3 | 7-21 |
| Lab | 7-22 |
| Lab 7-3: Extended Design Rules—Physical..... | 7-23 |
| Design Constraints..... | 7-27 |
| Property Assignments and Changes | 7-28 |
| DRC Marker Display | 7-29 |
| Lab | 7-30 |

| | |
|--|------|
| Lab 7-4: Working with Properties | 7-31 |
| Lesson 8: Component Placement..... | 8-1 |
| Design Layout Process | 8-2 |
| Prerequisites..... | 8-3 |
| Interactive Placement..... | 8-4 |
| Placement Grid..... | 8-5 |
| Strategy | 8-6 |
| Floorplanning with Rooms | 8-7 |
| Creating a Room | 8-8 |
| Assign RefDes Command..... | 8-9 |
| Labs..... | 8-10 |
| Lab 8-1: Floorplanning | 8-11 |
| Lab 8-2: Assigning Preplaced Packages | 8-16 |
| Placement-Related Properties | 8-17 |
| Placement Commands | 8-18 |
| Manual Placement Commands | 8-19 |
| Changing the Default Orientation..... | 8-20 |
| Lab | 8-21 |
| Lab 8-3: Manual Placement | 8-22 |
| Quickplace | 8-28 |
| Deleting Components | 8-30 |
| Labs..... | 8-31 |
| Lab 8-4: Using Quickplace | 8-32 |
| Lab 8-5: Removing Components from the Board..... | 8-40 |
| Lesson 9: Advanced Placement | 9-1 |
| Ratsnest..... | 9-2 |
| Automatic Swapping of Functions and Pins..... | 9-3 |
| Automatic Swap..... | 9-4 |
| Running Automatic Swap | 9-5 |
| Interactive Swap..... | 9-6 |
| Selecting Alternate Packages..... | 9-7 |
| Updating Symbols in a Design | 9-9 |
| Updating Padstacks..... | 9-10 |
| Modifying Padstacks | 9-12 |
| Creating a Library from a Design..... | 9-13 |
| Cross Placement with DE HDL..... | 9-14 |
| Cross Selection with DE CIS..... | 9-15 |
| Cross Highlighting between PCB Editor and DE CIS..... | 9-16 |
| Labs..... | 9-17 |
| Lab 9-1: Displaying Ratsnests | 9-18 |
| Lab 9-2: Swapping Components, Pins, and Functions | 9-20 |
| Lab 9-3: Advanced Placement with ALT_SYMBOL (Optional)..... | 9-23 |
| Lab 9-4: Using the DE HDL Schematic for Manual Placement (Optional) | 9-26 |
| Lab 9-5: Using the DE CIS Schematic for Manual Placement (Optional) | 9-30 |
| Lesson 10: Routing and Glossing | 10-1 |
| Design Layout Process | 10-2 |
| Accessing Interactive Routing Modes | 10-3 |
| Routing Grids: Fixed..... | 10-4 |

| | |
|--|-------|
| Routing Grids: Variable | 10-5 |
| Finding Nets or Reviewing Rats..... | 10-6 |
| Adding Signal Connections | 10-7 |
| Inserting Vias..... | 10-8 |
| Selecting Via Types | 10-9 |
| Define Blind/Buried Via..... | 10-10 |
| Auto Define Blind/Buried Via..... | 10-11 |
| Pop-Up Menu Options..... | 10-13 |
| Options Form..... | 10-14 |
| Options Form—Smooth..... | 10-15 |
| Options Form—Bubble/Gridless | 10-16 |
| Labs | 10-17 |
| Lab 10-1: Defining Etch Grids | 10-19 |
| Lab 10-2: Adding and Deleting Connect Lines and Vias..... | 10-21 |
| Accessing the PCB Router | 10-28 |
| Autoroute Prerequisites | 10-28 |
| Preparing for Automatic Routing | 10-29 |
| The PCB Editor-PCB Router Process | 10-30 |
| Labs | 10-31 |
| Lab 10-3: Preparing for Autorouting | 10-32 |
| Lab 10-4: Using the PCB Router..... | 10-37 |
| Editing Existing Etch..... | 10-40 |
| Moving Etch with the Slide Option..... | 10-41 |
| Editing Vertices | 10-42 |
| Changing the Layer or Width of a Connection..... | 10-43 |
| Deleting Etch | 10-44 |
| Using the Cut Option..... | 10-45 |
| Interactive Routing Properties | 10-46 |
| Glossing the Design..... | 10-47 |
| Labs | 10-48 |
| Lab 10-5: Checking for Unconnected Pins..... | 10-49 |
| Lab 10-6: Improving Routed Connections | 10-51 |
| Lab 10-7: Replacing Etch and Using the Cut Option | 10-54 |
| Lab 10-8: Running Gloss..... | 10-57 |
| Lesson 11: Copper Areas and Positive or Negative Planes | 11-1 |
| Design Layout Process | 11-2 |
| Copper Area Images | 11-3 |
| Adding a Copper Area..... | 11-4 |
| Global Dynamic Parameters - Shape Fill..... | 11-6 |
| Global Dynamic Parameters - Void Controls | 11-7 |
| Global Dynamic Parameters - Clearances | 11-8 |
| Global Dynamic Parameters - Thermal Relief Connects..... | 11-9 |
| Adding Copper Shapes..... | 11-10 |
| Editing Copper Shapes..... | 11-11 |
| Lab | 11-12 |
| Lab 11-1: Copper Areas..... | 11-13 |
| Lesson 12: Preparing for Post Processing | 12-1 |
| Design Layout Process | 12-2 |
| Renaming Reference Designators | 12-3 |

| | |
|--|-------|
| Rename Reference Designators (Main Form)..... | 12-4 |
| Rename Reference Designators (Setup Form)..... | 12-6 |
| Rename Reference Designators—Key Points..... | 12-7 |
| Backannotation | 12-8 |
| Backannotation Examples | 12-9 |
| Backannotation—DE HDL Export Netlist..... | 12-10 |
| Backannotation to DE HDL..... | 12-11 |
| Property Backannotation..... | 12-12 |
| DE CIS Integrated Logic Design/Physical Layout | 12-13 |
| PCB Editor-DE CIS Backannotation | 12-14 |
| Third-Party Backannotation Process..... | 12-15 |
| Third-Party Backannotation | 12-16 |
| Labs..... | 12-17 |
| Lab 12-1: Renaming Components | 12-18 |
| Lab 12-2: PCB Editor to DE HDL Backannotation | 12-22 |
| Lab 12-3: PCB Editor to DE CIS Backannotation | 12-24 |
| Lab 12-4: PCB Editor Backannotation to a Third-Party Schematic DE CIS Tool..... | 12-25 |
| Lesson 13: Preparing the Board Design for Manufacturing | 13-1 |
| Design Layout Process | 13-2 |
| Creating Silkscreens | 13-3 |
| Creating Silkscreens—Menu | 13-4 |
| Incremental Update of Silkscreens..... | 13-5 |
| Generating Reports | 13-6 |
| Labs..... | 13-7 |
| Lab 13-1: Creating Silkscreens..... | 13-8 |
| Lab 13-2: Creating Reports..... | 13-11 |
| Creating Checkplots..... | 13-12 |
| Generating Artwork | 13-13 |
| Artwork Parameters | 13-14 |
| The Aperture File | 13-16 |
| Film Control..... | 13-17 |
| Film Options..... | 13-18 |
| Adding a Photoplot Outline | 13-20 |
| Generating Gerber Files..... | 13-21 |
| Viewing Gerber Files..... | 13-22 |
| Labs..... | 13-22 |
| Lab 13-3: Creating Artwork Files..... | 13-24 |
| Lab 13-4: Viewing Gerber Files | 13-31 |
| Creating Fabrication Drawings..... | 13-33 |
| Drill Symbols and Legend Table | 13-34 |
| Drill Customization Spreadsheet | 13-35 |
| Generating an NC Drill File | 13-36 |
| Creating the Parameters File | 13-37 |
| Creating Assembly Drawings | 13-39 |
| Labs..... | 13-40 |
| Lab 13-5: Creating a Drill Legend..... | 13-41 |
| Lab 13-6: Creating Fab and Assembly Drawings..... | 13-43 |
| Lab 13-7: Creating an NCDRILL File..... | 13-45 |
| Appendix A: File Extensions | A-1 |